CD4510B, CD4516B Types

CMOS Presettable Up/Down Counters

High-Voltage Types (20-Volt Rating)

CD4510B – – – BCD Type
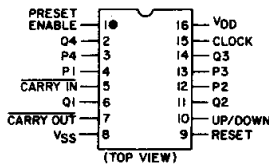
CD4516B – – – Binary Type

■ CD4510B Presettable BCD Up/Down Counter and the CD4516 Presettable Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The CD4510B will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode.

If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage.

The CD4510B and CD4516B can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage. (See Fig. 15).

These devices are similar to types MC14510 and MC14516.

The CD4510B and CD4516B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). The CD4516B types also are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix).

Features:

■ Medium-speed operation --
f_{CL} = 8 MHz typ. at 10 V

■ Synchronous internal carry propagation

■ Reset and Preset capability

■ 100% tested for quiescent current at 20 V

■ 5-V, 10-V, and 15-V parametric ratings

■ Standardized symmetrical output characteristics

■ Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C

■ Noise margin (full package-temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V·
  2.5 V at V_{DD} = 15 V

■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

CD4510B, CD4516B FUNCTIONAL DIAGRAM

92CS-24824
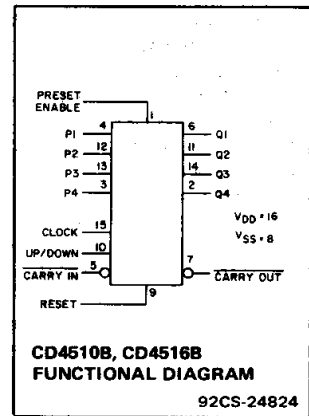
Applications:

■ Up/Down difference counting

■ Multistage synchronous counting

■ Multistage ripple counting

■ Synchronous frequency dividers

CD4510B, CD4516B
TERMINAL ASSIGNMENT
92CS-27015

OPERATING CONDITIONS AT T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (At T_A = Full Package-Temperature Range)		3	18	V
Clock Pulse Width, t_W	5	150	–	ns
	10	75	–	
	15	60	–	
Clock Input Frequency, f_{CL}	5	–	2	MHz
	10	–	4	
	15	–	5.5	
Preset Enable or Reset Removal Time●	5	150	–	ns
	10	80	–	
	15	60	–	
Clock Rise and Fall Time, t_rCL, t_fCL *	5	–	15	μs
	10	–	5	
	15	–	5	
Carry-In Setup Time, t_S	5	130	–	ns
	10	60	–	
	15	45	–	
Up-Down Setup Time, t_S	5	360	–	ns
	10	160	–	
	15	110	–	
Preset Enable or Reset Pulse Width, t_W	5	220	–	ns
	10	100	–	
	15	75	–	

●Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time).

*If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

COMMERCIAL CMOS HIGH VOLTAGE ICs 3

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) .... −0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT .... ±10mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = −55°C to +100°C 500mW

For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) .... −55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) .... −65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

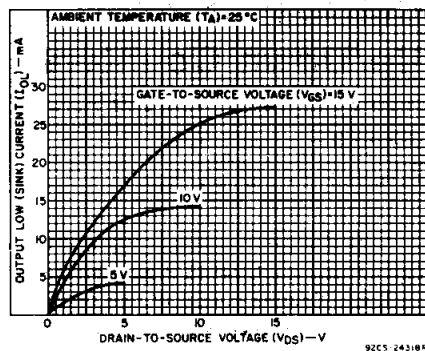At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

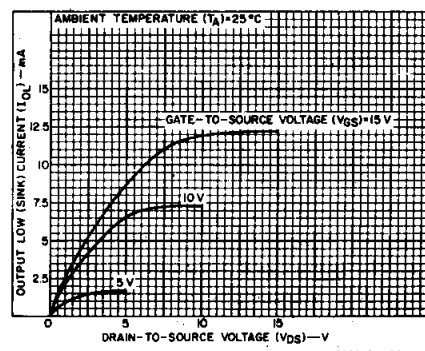Fig.1 − Typical output low (sink) current characteristics.

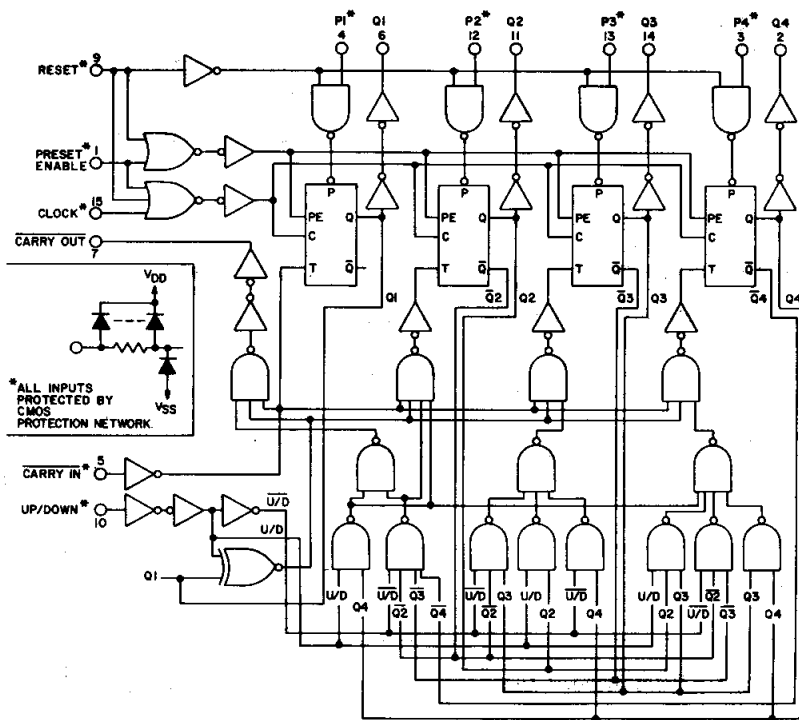Fig.2 − Minimum output low (sink) current characteristics.
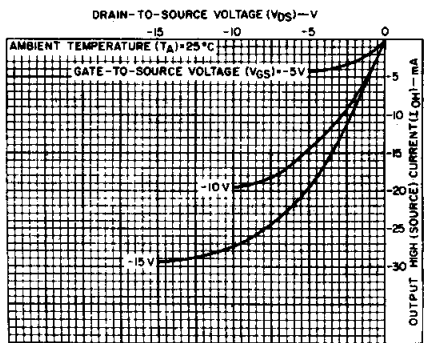

Fig.3 − Logic Diagram for CD4510B.

Fig.4 − Typical output high (source) current characteristics.
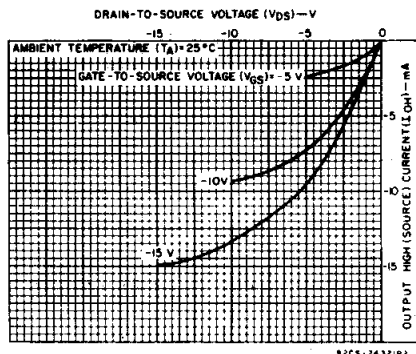

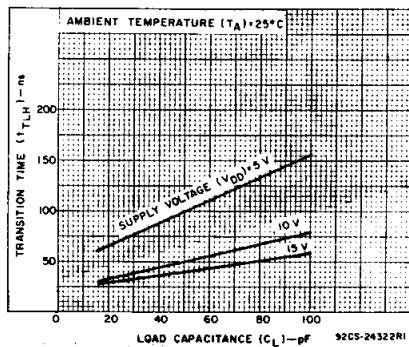Fig.5 − Minimum output high (source) current characteristics.

Fig.6 − Typical transition time vs. load capacitance.
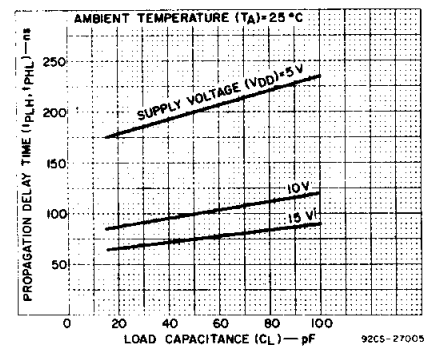

Fig.7 − Typical propagation delay time vs. load capacitance for clock-to-Q outputs.

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)				+25			UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	V
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	V
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	±10^{-5}	±0.1	μA
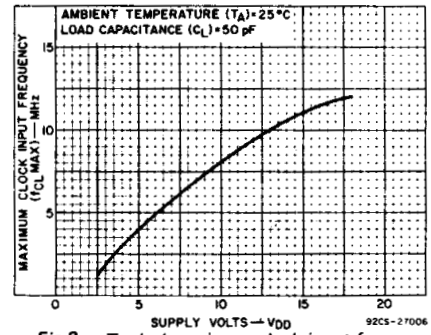
Fig.8 – Typical maximum clock input frequency vs. supply voltage.
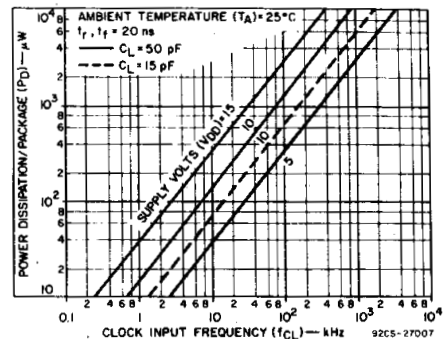
Fig.9 – Typical dynamic power dissipation vs. frequency.

3

COMMERCIAL CMOS HIGH VOLTAGE ICs
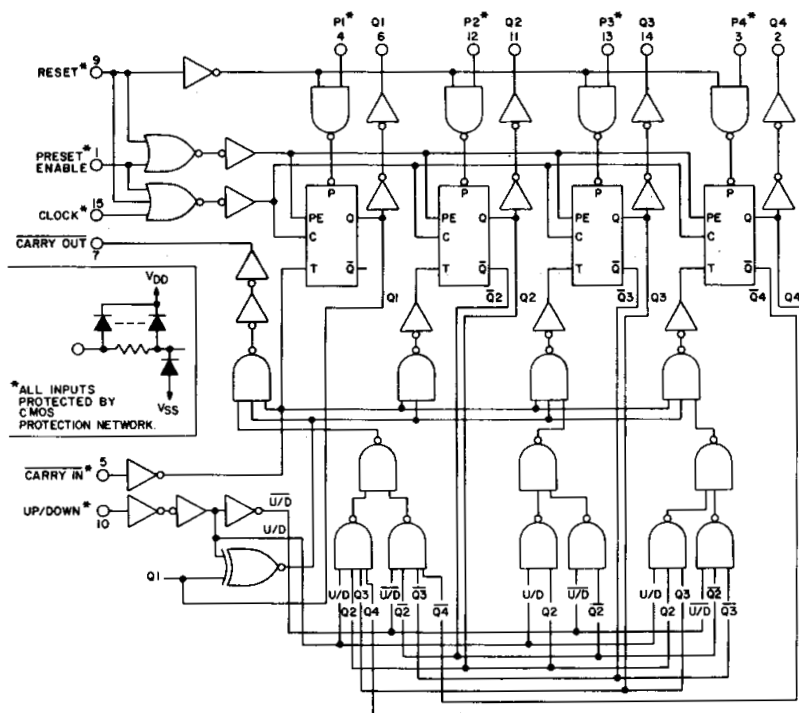

Fig. 10 – Logic Diagram for CD4516B.

92CL-27004R2
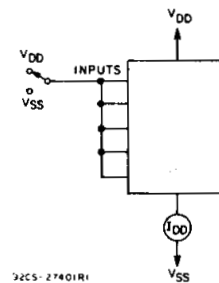
Fig. 11 – Quiescent-device-current test circuit.

NOTE:
MEASURE INPUTS SEQUENTIALLY.
TO BOTH V_{DD} AND V_{SS}.
CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}.
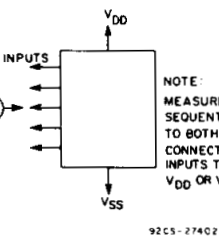
92CS-27402

Fig. 12 – Input-current test circuit.

CD4510B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $C_L = 50$ pF,
Input t_r, $t_f = 20$ ns, $R_L = 200$ kΩ

Characteristic	Conditions V_{DD} (V)	Limits All Packages Min.	Typ.	Max.	Units
Propagation Delay Time (t_{PHL}, t_{PLH}):					
Clock-to-Q Output (See Fig. 10)	5	—	200	400	
	10	—	100	200	ns
	15	—	75	150	
Preset or Reset-to-Q Output	5	—	210	420	
	10	—	105	210	ns
	15	—	80	160	
Clock-to-Carry Out	5	—	240	480	
	10	—	120	240	ns
	15	—	90	180	
Carry-In-to-Carry Out	5	—	125	250	
	10	—	60	120	ns
	15	—	50	100	
Preset or Reset-to-Carry Out	5	—	320	640	
	10	—	160	320	ns
	15	—	125	250	
Transition Time (t_{THL}, t_{TLH}) (See Fig. 9)	5	—	100	200	
	10	—	50	100	ns
	15	—	40	80	
Max. Clock Input Frequency (f_{CL})	5	2	4	—	
	10	4	8	—	MHz
	15	5.5	11	—	
Input Capacitance (C_{IN})		—	5	7.5	pF
Set-up Time, t_S Preset Enable to J_n	5	25	12	—	
	10	10	6	—	
	15	10	5	—	
Hold times, t_H Clock to Carry-In	5	60	30	—	
	10	30	4	—	
	15	30	1	—	ns
Clock to Up/Down	5	30	10	—	
	10	30	4	—	
	15	30	5	—	
Preset Enable to J_n	5	70	35	—	
	10	40	20	—	
	15	40	20	—	

NOTE:
TEST ANY ONE INPUT,
WITH OTHER INPUTS AT
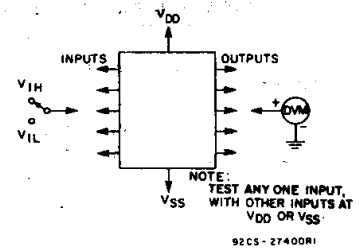V_{DD} OR V_{SS}.

92CS-27400RI
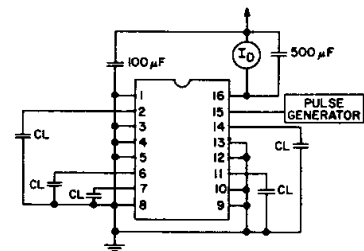
Fig. 13 — Input-voltage test circuit.

92CM-27012

Fig. 14 — Power-dissipation test circuit and input waveform.
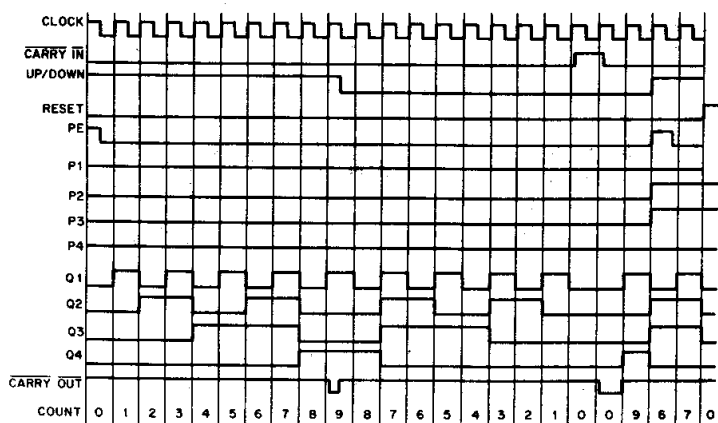
Fig. 15 — Timing Diagram for CD4510B.

92CM-27008

CL	CI	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
⌐	0	1	0	0	COUNT UP
⌐	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

X = DON'T CARE

TRUTH TABLE

92CS-27037RI

Dimensions and Pad Layout for CD4510BH.
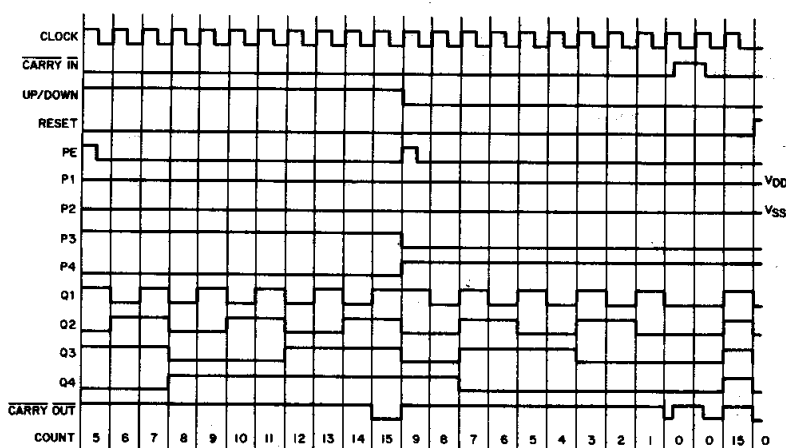
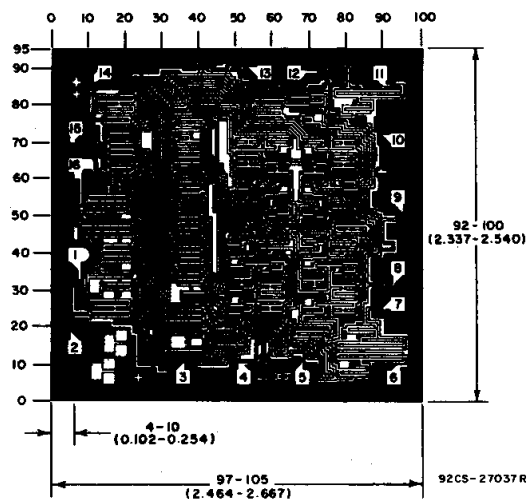Fig. 16 — Timing diagram for CD4516B.

92CM-27009RI

92CS-27036RI

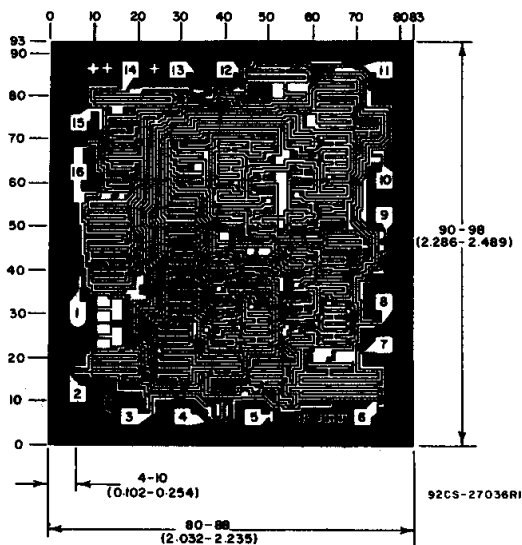Dimensions and Pad Layout for CD4516BH.

92CS-27014
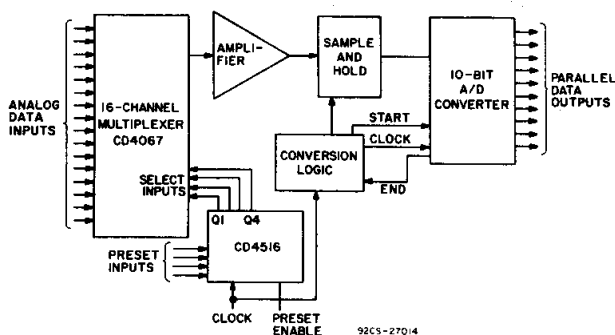
This acquisition system can be operated in the random access mode by jamming in the channel number at the present inputs, or in the sequential mode by clocking the CD4516B.

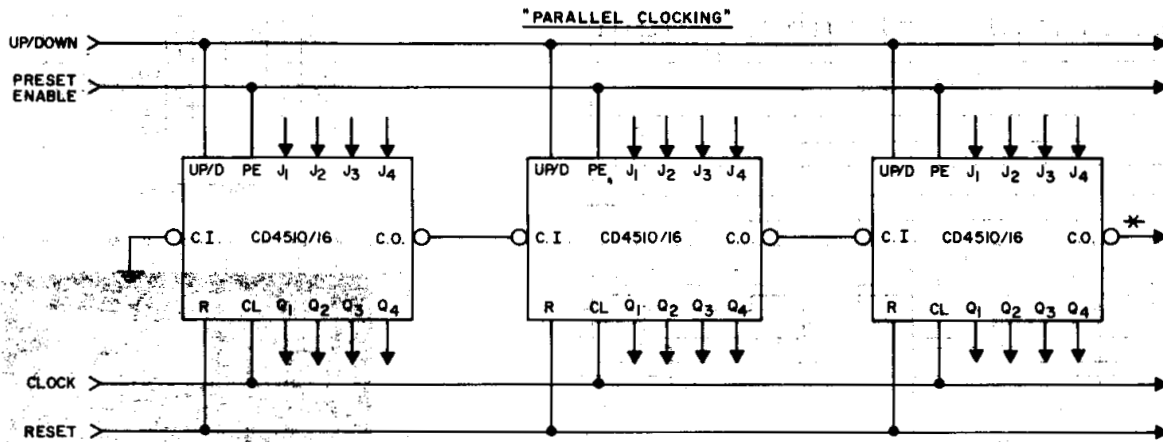Fig. 17 — Typical 16-channel, 10-bit data acquisition system.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CD4510B Types

"PARALLEL CLOCKING"

UP/DOWN

PRESET
ENABLE

CLOCK

RESET

* CARRY OUT lines at the 2nd, 3rd, etc., stages may have a negative-going glitch pulse resulting from differential delays of different CD4510/16 IC's. These negative-going glitches do not affect proper CD4510/16 operation. However, if the CARRY OUT signals are used to trigger other edge-sensitive logic devices, such as FF's or counters, the CARRY OUT signals should be gated with the clock signal using a 2-input OR gate such as CD4071B.

"RIPPLE CLOCKING"

UP/DOWN

PRESET
ENABLE

CLOCK

RESET

1/4 CD4071B
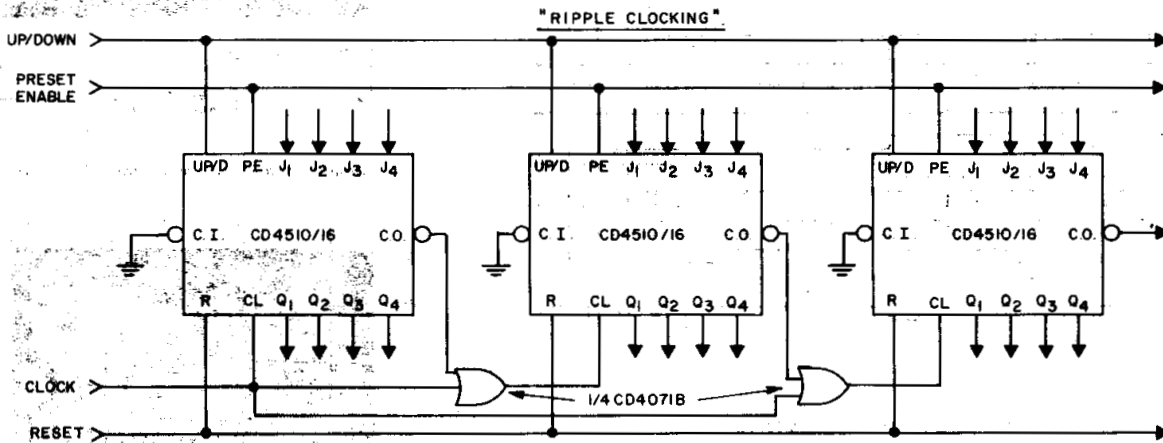
RIPPLE CLOCKING MODE:
THE UP/DOWN CONTROL CAN BE CHANGED AT ANY COUNT. THE ONLY RESTRICTION ON CHANGING THE UP/DOWN CONTROL IS THAT THE CLOCK INPUT TO THE FIRST COUNTING STAGE MUST BE "HIGH".

For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages, and CO is connected directly to the CL input of the next stage with CI grounded.

92CL-17194R5

Fig. 18 — Cascading counter packages.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4510BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4510BE	Samples
CD4510BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4510BE	Samples
CD4510BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4510B	Samples
CD4510BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4510B	Samples
CD4510BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM510B	Samples
CD4516BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4516BE	Samples
CD4516BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4516BE	Samples
CD4516BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4516BF	Samples
CD4516BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4516BF3A	Samples
CD4516BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4516B	Samples
CD4516BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM516B	Samples
CD4516BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM516B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4516B, CD4516B-MIL :

- Catalog: CD4516B

- Military: CD4516B-MIL

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4510BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4510BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4516BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4516BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4510BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD4510BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4516BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD4516BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°–15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) M

14/18 Pin Only
20 Pin vendor option

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

16   9

Ⓓ 4,50
    4,30

6,60
6,20

1   8

5,10
4,90

Ⓒ

0,15 NOM

Gage Plane

0,25

0°−8°

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ 0,10
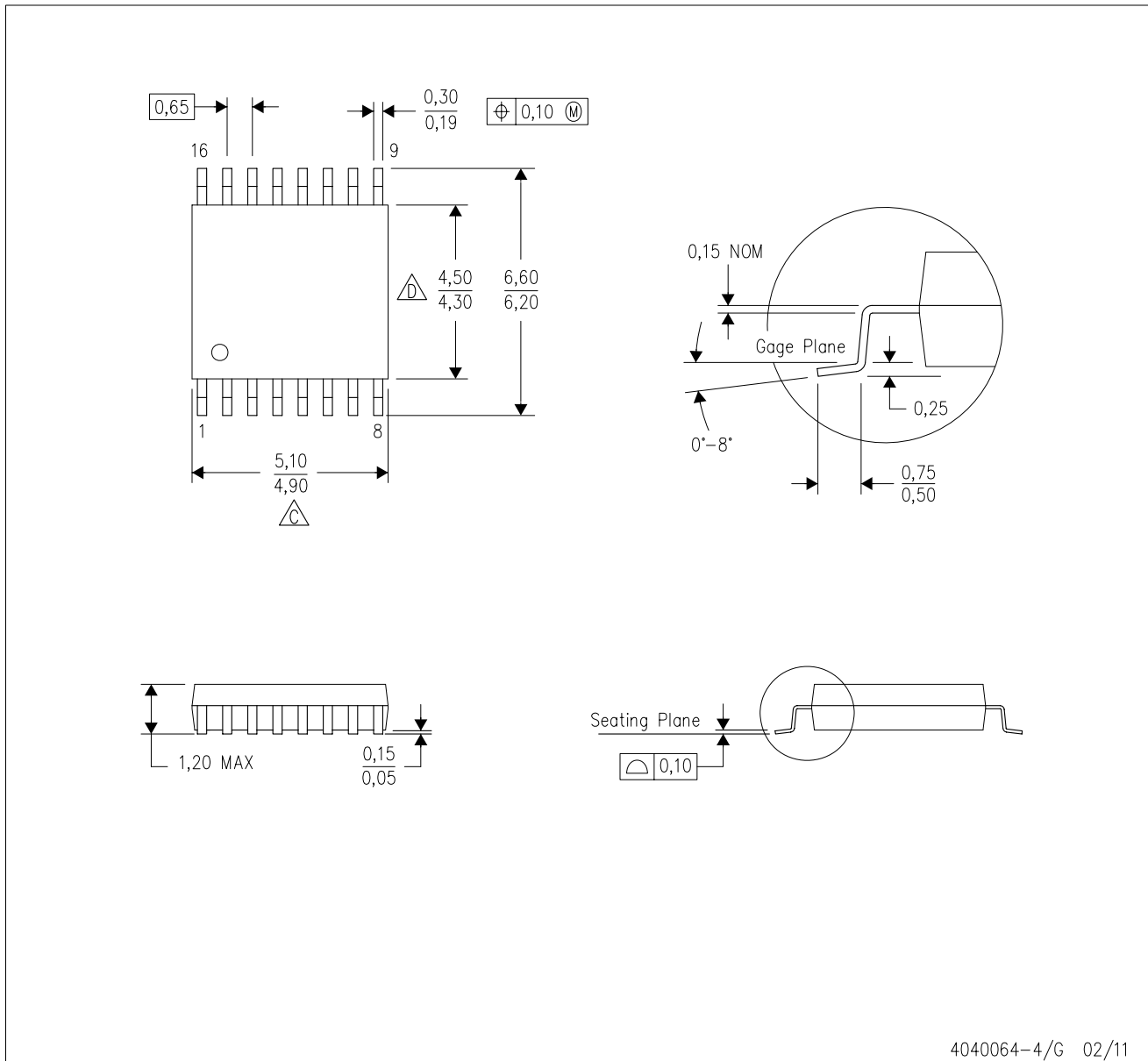
4040064−4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B. This drawing is subject to change without notice.
          Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
          Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E. Falls within JEDEC MO−153

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PW (R–PDSO–G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

←— 14x0,65

5,60

Stencil Openings
(Note D)

←— 16x0,30

←— 14x0,65

16x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

←— 0,35

1,60

Example
Solder Mask Opening
(See Note E)

←— 0,07
All Around
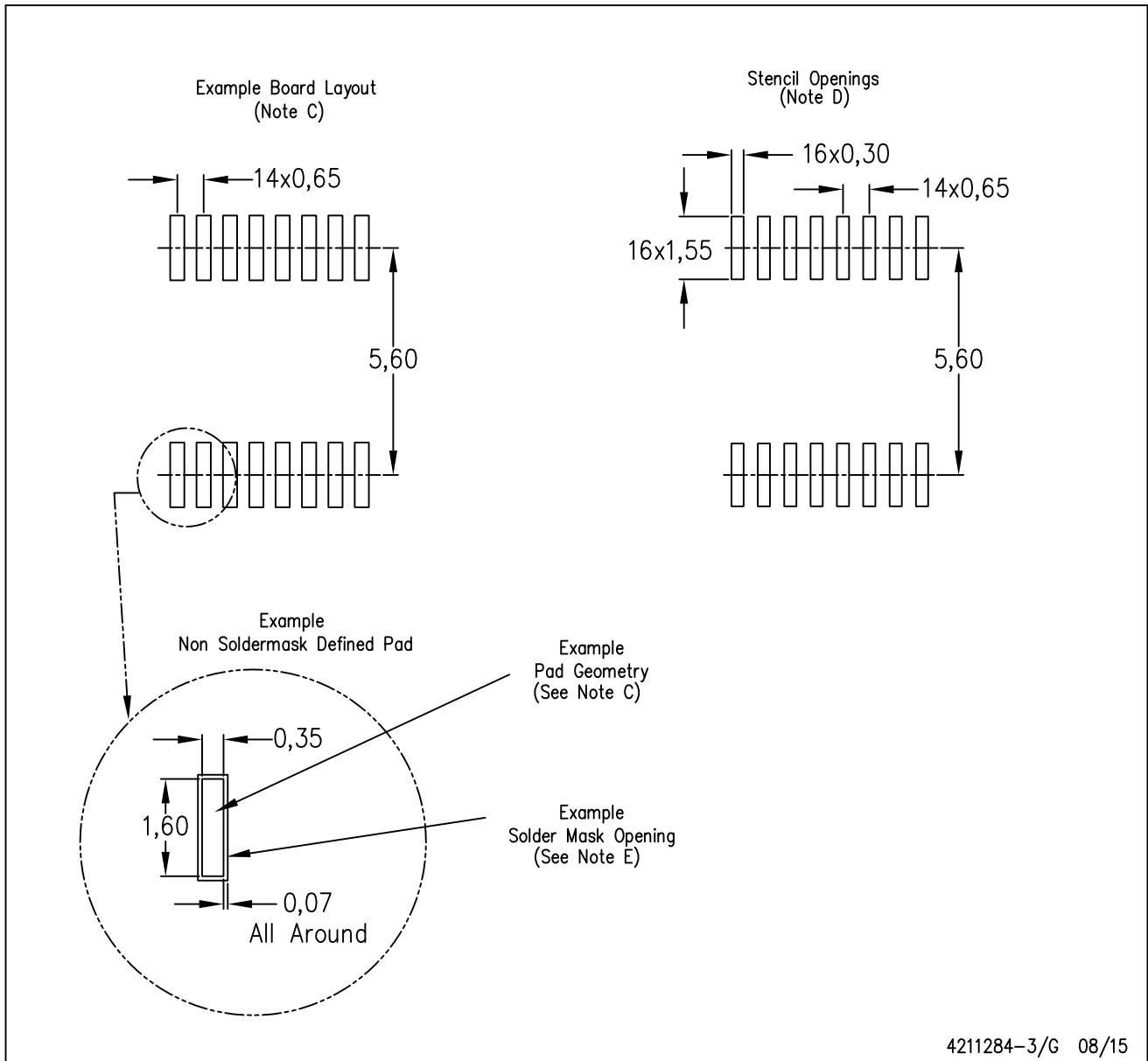
4211284–3/G   08/15

NOTES: A.   All linear dimensions are in millimeters.
            B.   This drawing is subject to change without notice.
            C.   Publication IPC–7351 is recommended for alternate designs.
            D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
                contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
            E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

	PINS **	14	16	20	24
DIM					
A MAX		10,50	10,50	12,90	15,30
A MIN		9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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